TSMC-02-218

January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/689,431 10/20/03

Hung-Der Su et al.

A METHOD FOR MEASURING CAPACITANCE-VOLTAGE CURVES FOR TRANSISTORS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

"Gate Dielectric Capacitance-Voltage Characterization Using the Model 4200 Semiconductor Characterization System," Keithley, Application Note Series, No. 2239, discusses maintaining the quality and reliability of gate oxides.

Agilent Technologies Impedance Measurement Handbook, 2nd Edition, Application Note 5950, staff, Agilent Technologies Co. Ltd, Palo Alto, CA, Copyright 2000, 5-12 to 5-14, illustrates a capacitance-voltage test system.

"Evaluation of Gate Oxides Using a Voltage Step Quasi-Static CV Method," Application Note 4156-10, Agilent Technologies, pp. 1-4, discusses Agilent 4155C/4156C semiconductor parameter analyzer.

"MOS Capacitance Measurements for High-Leakage Thin Dielectrics," Yang et al., IEEE Transactions On Electron Devices, Vol. 46, No. 7, July 1999, pp. 1500-1501, presents a technique, which allows the frequency-independent device capacitance to be accurately extracted from impedance measurements at two frequencies.

U.S. Patent 5,485,097 to Wang, "Method of Electrically Measuring a Thin Oxide Thickness by Tunnel Voltage," discusses a method of electrically measuring a thin oxide thickness by tunnel voltage.

U.S. Patent 6,456,105 to Tao, "Method for Determining Transistor Gate Oxide Thickness," describesa method for determining the electrical thickness of a very thin gate oxide layer of a MOS transistor that is subject to relatively high leakage current owing to its thinness.

"MOS C-V Characterization of Ultrathin Gate Oxide Thickness (1.3-1.8 nm)", Choi et al., IEEE Electron Device Letters, Vol. 20, No. 6, June 1999, pp. 292-294, describes an equivalent circuit approach to MOS capacitance-voltage (C-V) modeling of ultra-thin gate oxides (1.3-1.8nm).

U.S. Patent 6,472,236 to Wang et al., "Determination of Effective Oxide Thickness of a Plurality of Dielectric Materials in a MOS Stack," describes a system and method for determining an effective oxide thickness for each of first and second dielectric structures that form a MOS (metal oxide semiconductor) stack.

U.S. Patent 6,066,952 to Nowak et al., "Method for Polysilicon Crystalline Line Width Measurement Post Etch in Undoped-poly Process," discusses a method for measurement of a width of an undoped or lightly diped polysilicon line.

U.S. Patent 5,793,675 to Cappelletti et al., "Method of Evaluating the Gate Oxide of Non-Volatile EPROM, EEPROM and Flash-EEPROM Memories," describes a method for evaluating the gate oxide on non-volatile EPROM, EEPROM and flash-EEPROM memories.

U.S. Patent 6,339,339 to Maeda, "TFT and Reliability Evaluation Method Thereof," describes a method for evaluating the reliability of a thin film transistor (TFT), time coefficient, voltage coefficient and temperature coefficient are experimentally produced from megative bias thermal stress tests.

U.S. Patent 6,472,233 to Ahmed et al., "MOSFET Test Structure for Capacitance-Voltage Measurements," teaches a MOS transistor test structure for capacitance-voltage measurements.

U.S. Patent 6,011,404 to Ma et al., "System and Method for Determining Near-surface Lifetimes and the Tunneling Field of a Dielectric in a Semiconductor," reveals a system and method for determining near-surface lifetimes and the tunneling field of a dielectric in a semiconductor.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-218	10/689,431
Applicant: Hung-Der Su et al.	
Filing Date: 10/20/03	Group Art Unit:

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5485097	1/16/96	Wang	324	765	8/8/94
	6456105	9/24/02	Tao	324	769	8/8/00
	6472236	10/29/02	Wang et al.	438	14	7/13/01
	6066952	5/23/00	Nowak et al.	324	458	9/25/97
	5793675	8/11/98	Cappelletti et al.	365	185.09	4/1/97
	6339339	1/15/02	Maeda	324	769	1/22/01
	6472233	10/29/02	Ahmed et al.	438	14	6/5/00
	6011404	1/4/00	Ma et al.	324	765	7/3/97

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
	"Gate Dielectric Capacitance-Voltage Characterization Using the Model 4200 Semiconductor Characterization System", Keithley, Application Notes Series, No. 2239.
	Agilent Technologies Impedance Measurement Handbook, 2nd Edition, Application Note 5950, staff, Agilent Technologies Co. Ltd., Palo Alto, CA, Copyright 2000, 5-12 to 5-14.

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- "Evaluation of Gate Oxides Using a Voltage Step Quasi-Static CV Method," Application Note 4156-10, Agilent Technologies, pp. 1-4.
- "mos Capacitance Measurements for High-Leakage Thin Dielectrics, Vol. 46, No. 7, July 1999, pp. 1500-1501.
- "MOS C-V Characterization of Ultrathin Gate Oxide Thickness (1.3-1.8 nm)", Choi et al., IEEE Electron Device Letters, Vol. 20, No. 6, June 1999, pp. 292-294.

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